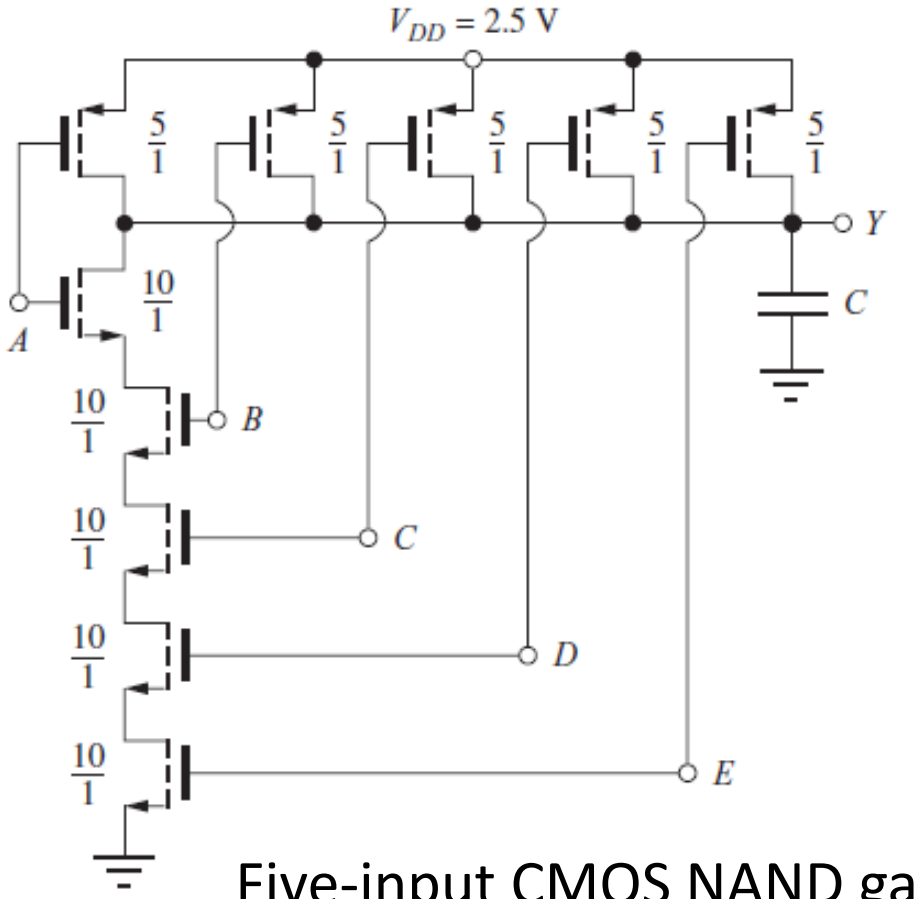
Announcements

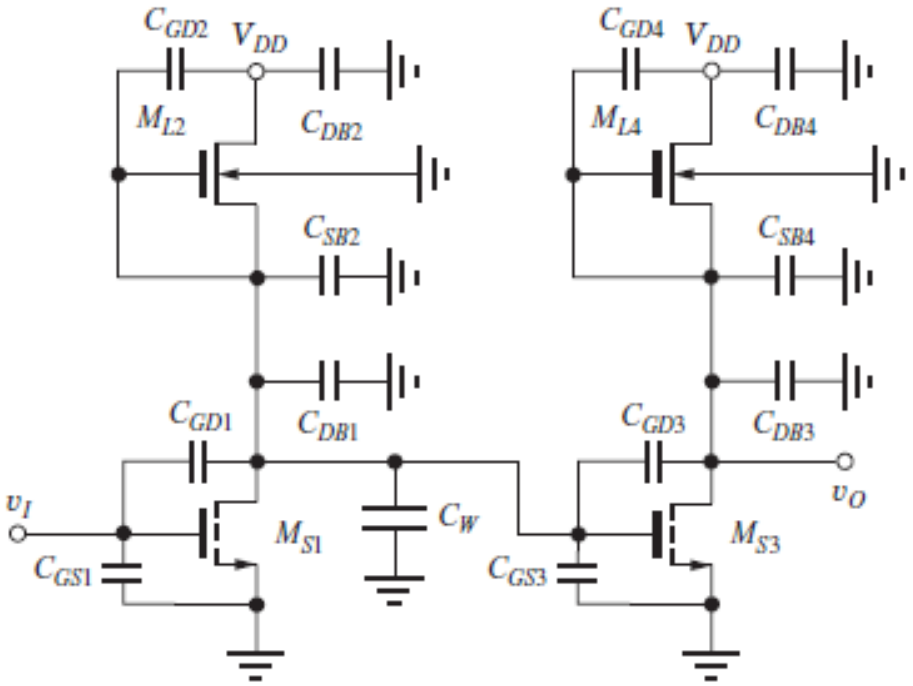
- Homework #8 due Friday.
- Exam solution posted.
  - Submit regrades by Friday in class.

Multi-Input CMOS NAND Gates

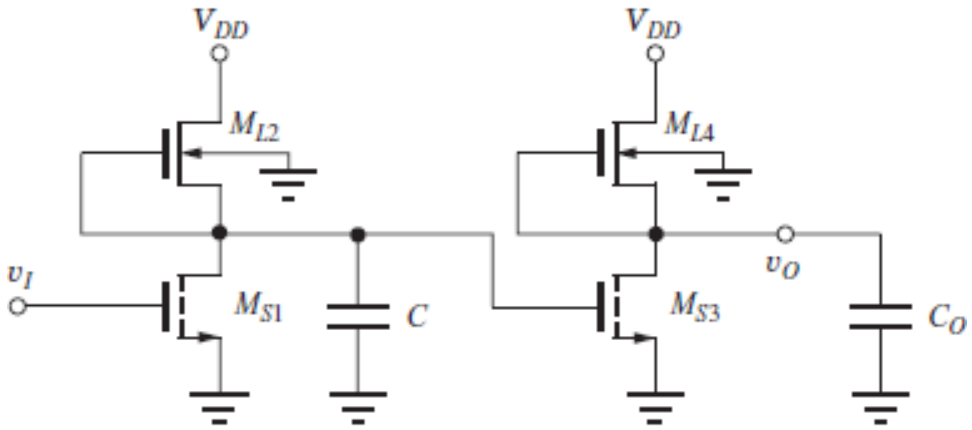


Five-input CMOS NAND gate: $Y = \overline{ABCDE}$

Capacitances in Logic Circuits

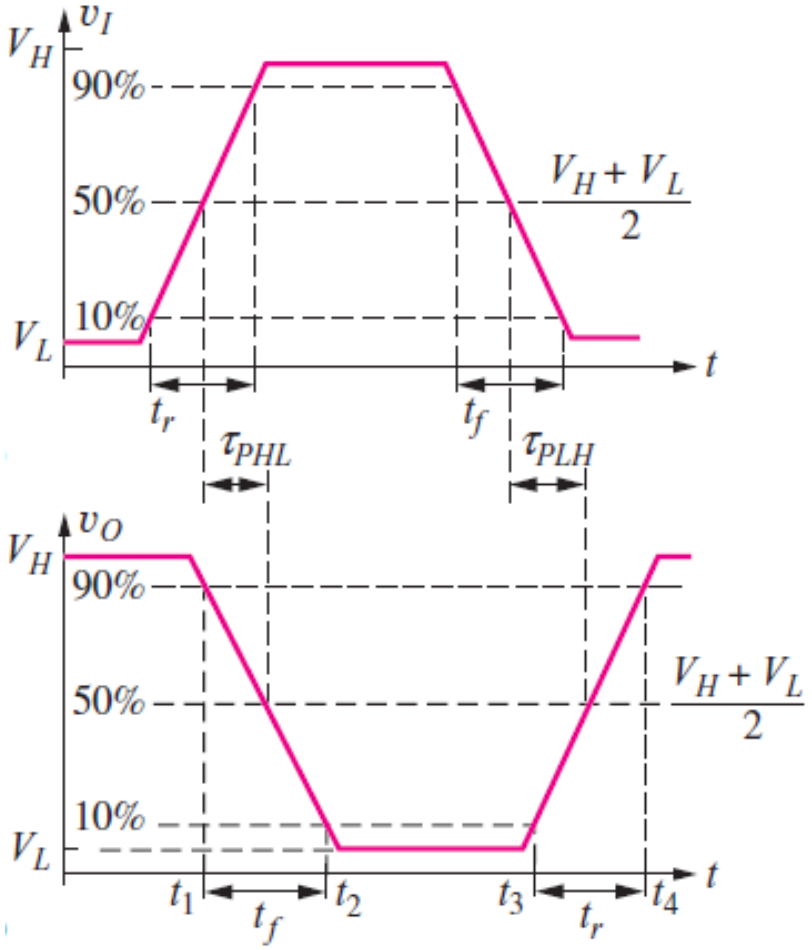


Various capacitances associated with transistors



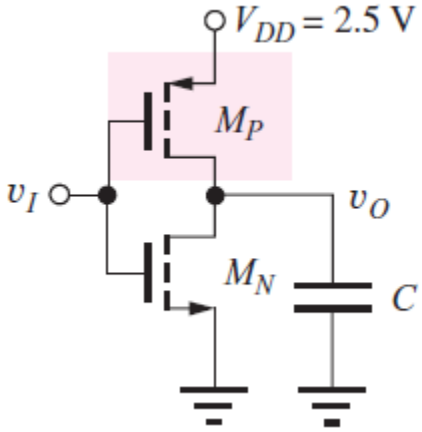
The capacitances on a given node can be lumped into a fixed effective nodal capacitance *C*

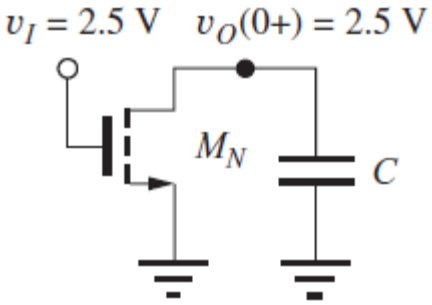
Logic Gate Dynamic Responses

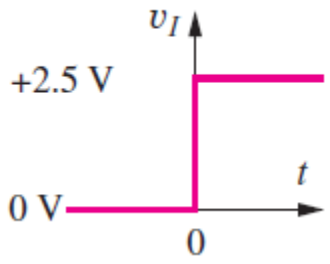


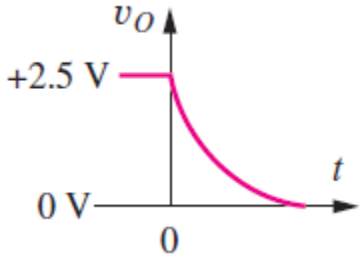
- **Rise time (t_r)**: time required from 10% point to 90% point
- **Fall time (t_f)**: time required from 90% point to 10% point
- **Propagation delay (τ_P)**: difference in time between the input and output signals reaching the 50% points
  - for output high-to-low: τ_{PHL}
  - for output low-to-high: τ_{PLH}
  - average propagation delay $\tau_P = (\tau_{PLH} + \tau_{PHL})/2$

Dynamic Response of CMOS Inverter







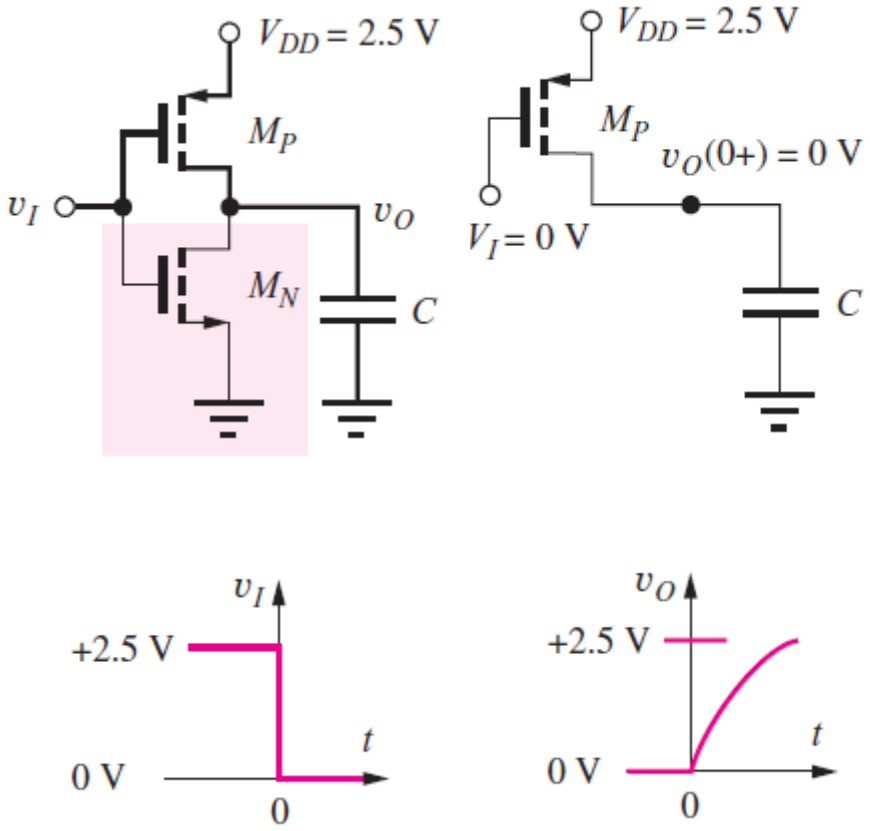


- Assume abrupt V_I change from V_L to V_H
- V_O changes from V_H to V_L by discharging C via M_N
- Same as the resistive load

$$\tau_{PHL} = 1.2 R_{onn} C$$

$$R_{onn} = \frac{1}{K_n (V_H - V_{TN})}$$

Dynamic Response of CMOS Inverter



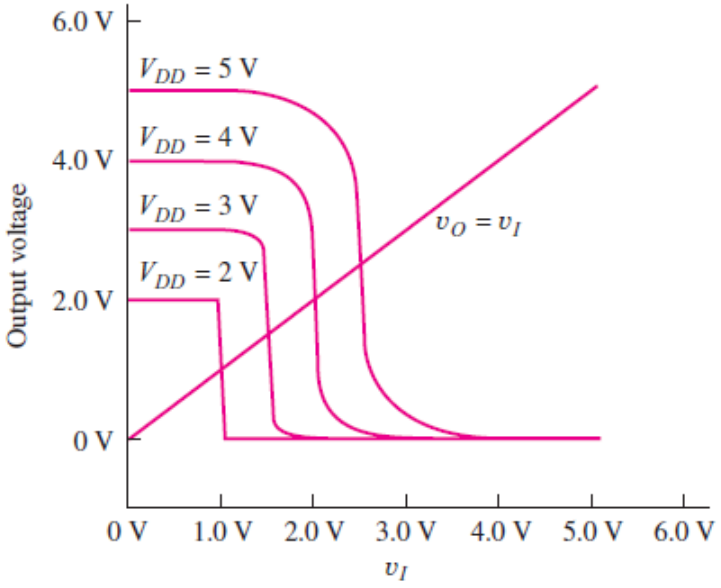
- Assume abrupt V_I change from V_H to V_L
- V_O changes from V_L to V_H by charging C via M_P
- Similarly we get

$$\tau_{PLH} = 1.2 R_{onp} C$$

$$R_{onp} = \frac{1}{K_p(V_H + V_{TP})}$$

CMOS Inverter with Symmetrical Delay

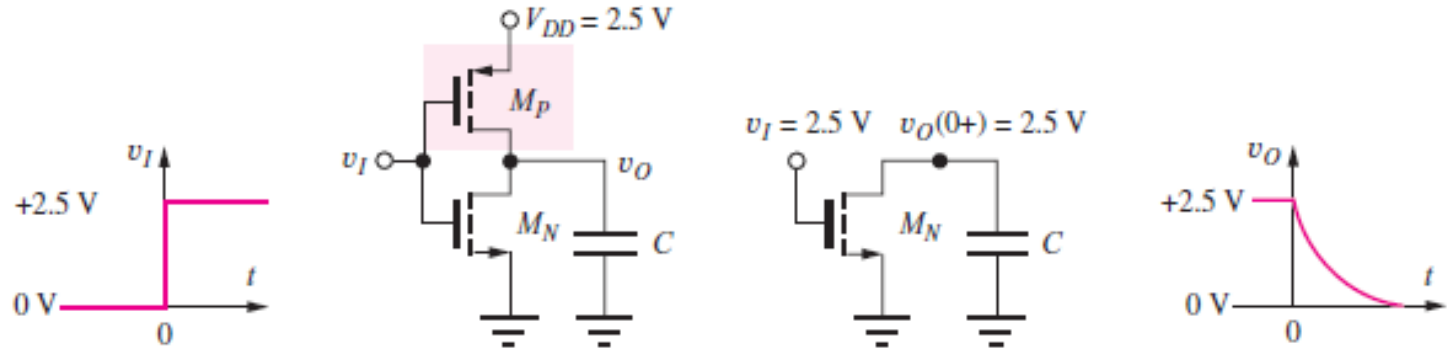
- CMS inverter with symmetrical delay has
  $\tau_{PLH} = \tau_{PHL} \Rightarrow R_{\text{on}n} = R_{\text{on}p} \Rightarrow K_n = K_p$
- This is exactly the "symmetrical" inverter



$$\mu_n = 2.5\mu_p \Rightarrow \left(\frac{W}{L}\right)_p = 2.5\left(\frac{W}{L}\right)_n$$

$$\tau_P = \frac{\tau_{PLH} + \tau_{PLH}}{2} = 1.2R_{\text{on}n}C$$

CMOS Switching Speed



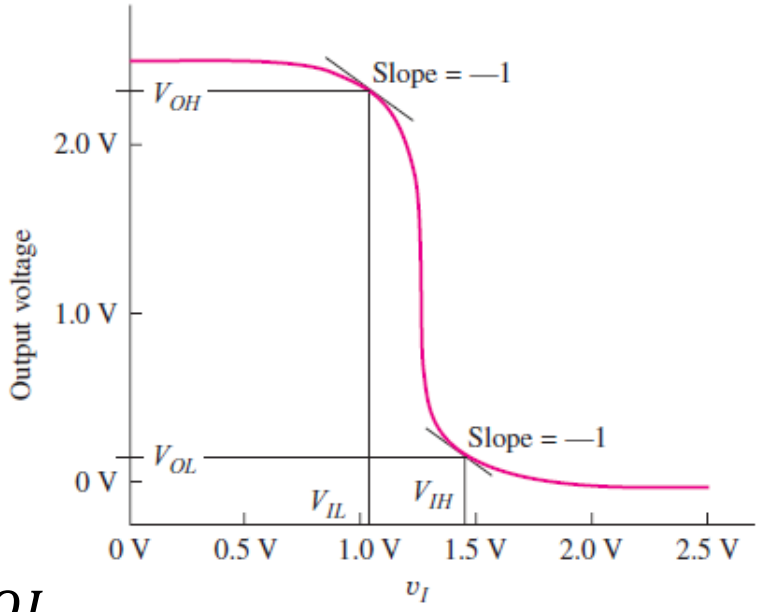
- Can estimate switching time for capacitive load very simply:

$$\Delta t = \frac{C_{\text{total}}\Delta v}{i_{\text{avg}}} = \frac{\Delta Q}{i_{\text{avg}}}$$

- For τ_{PHL}, v_I=V_{DD}, PMOS OFF, NMOS ON.
- NMOS saturated for $v_O > V_{DD}$-V_{TN}, linear for $v_O < V_{DD}$-V_{TN}
- Just the opposite for LH transition.

Symmetrical CMOS Inverter

- Symmetrical CMOS inverter:
  - $K_n = K_p, V_{Tn} = -V_{Tp} = V_T$
  - $\tau_{PLH} = \tau_{PHL}, R_{\text{on}n} = R_{\text{on}p}$
- If $V_T < V_{DD}/2$
  - $V_{OL} = \frac{V_{DD}}{8} - \frac{V_T}{4}, V_{OH} = V_{DD} - V_{OL}$
  - $V_{IL} = \frac{3V_{DD}}{8} + \frac{V_T}{4}, V_{IH} = V_{DD} - V_{IL}$
  - $NM_L = NM_H = \frac{V_{DD}}{4} + \frac{V_T}{2}$

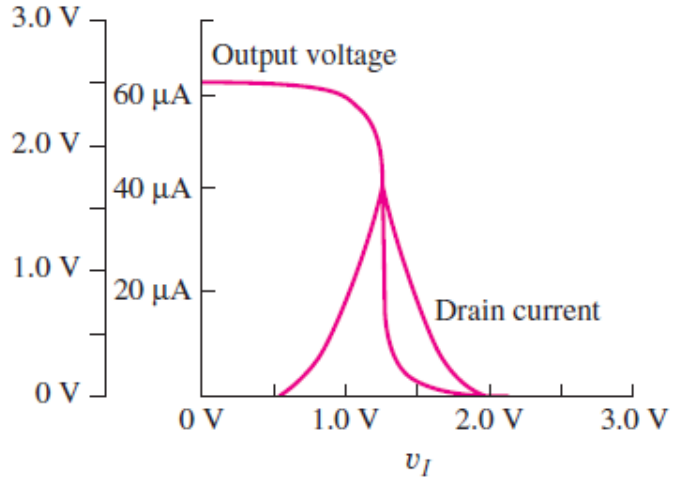


CMOS Performance Scaling

- $\tau_P = \frac{\tau_{PHL}+\tau_{PLH}}{2}$
  - $\tau_P \propto C$
  - $\tau_P \propto R_{\text{on}} \propto \left(\frac{W}{L}\right)^{-1}$
- Delay is proportional to total load capacitance *C*, and inversely proportional to W/L.
- Larger size (larger W/L) => shorter delay

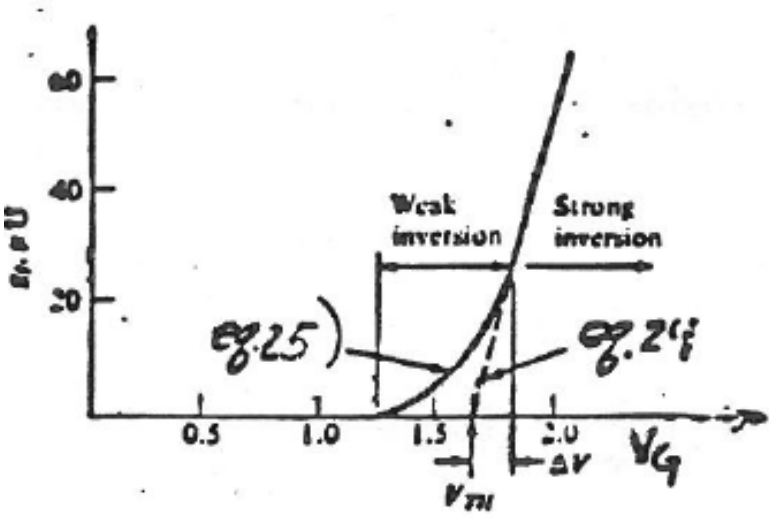
Power Dissipation

- Switching: CV_{DD}^2 per cycle
- Transition conduction: when $V_{TN} < v_{in} < V_{DD}+V_{TP}$, both transistors are on.
  - Depends on amount of time with $v_{in} \sim V_{DD}/2$ (t_r, t_f).
  - Can be 20-30% of CV_{DD}^2



- Subthreshold conduction: small currents even when devices are "off."

Subthreshold Conduction



Note that the linear relationship between g_I and $V_G - V_{th}$ agrees with experiment except for V_G very close to V_{th}.

$$Q_I' \cong -WC_{ox}^{"}(V_{GS} - V_T) \qquad [24]$$

$$Q_I' \cong -WC_{ox}^{"}\Delta V \exp\left(\frac{V_{GS} - V_T - \Delta V}{\Delta V}\right) \qquad [25]$$

Subthreshold slope
(1+α)60 mV/decade
Typical is 70-100 mV/dec

$$\Delta V = (1+\alpha)\frac{kT}{q} = \left(1 + \frac{C_d^{"}}{C_{ox}^{"}}\right)\frac{kT}{q}$$

Subthreshold Conduction

$$Q_I' \cong -WC_{ox}^{"}\Delta V \exp\left(\frac{V_{GS}-V_T-\Delta V}{\Delta V}\right)$$

$$\Delta V = (1+\alpha)\frac{kT}{q} = \left(1+\frac{C_d^{"}}{C_{ox}^{"}}\right)\frac{kT}{q}$$

$$i_{Dsub} = \left(\frac{Q_I'}{L}\right)\mu\frac{kT}{q}\left(1-e^{-qv_{DS}/kT}\right)$$

Subthreshold slope
(1+α)60 mV/decade
Typical is 70-100 mV/dec
(60 mV/dec for $\alpha = 0$)

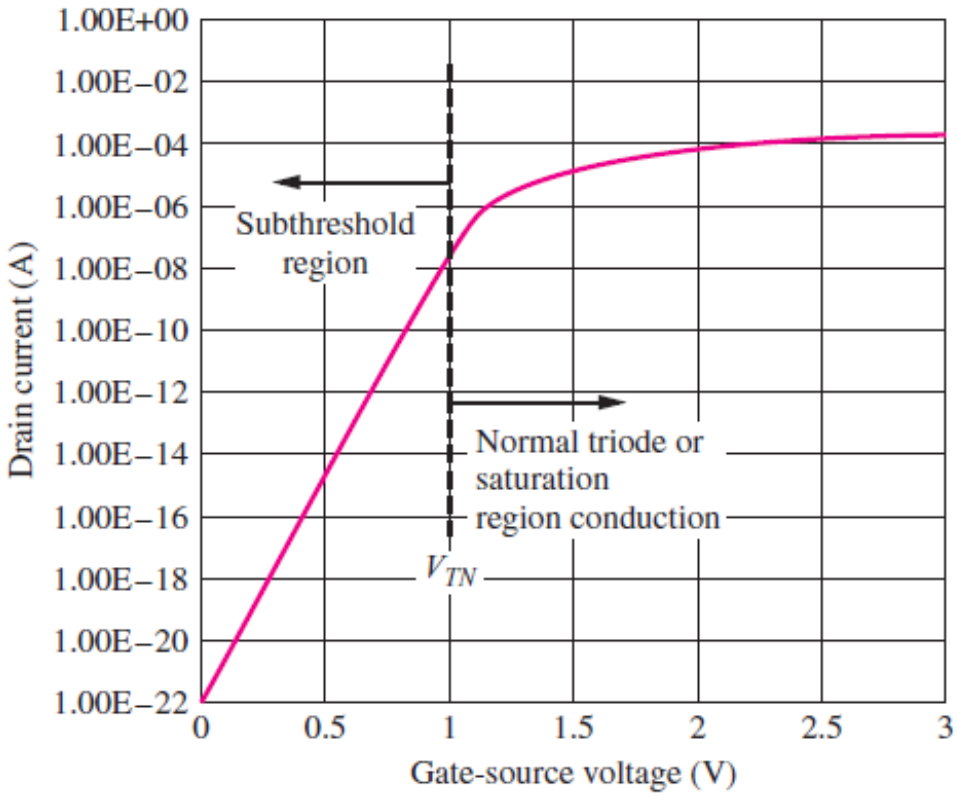
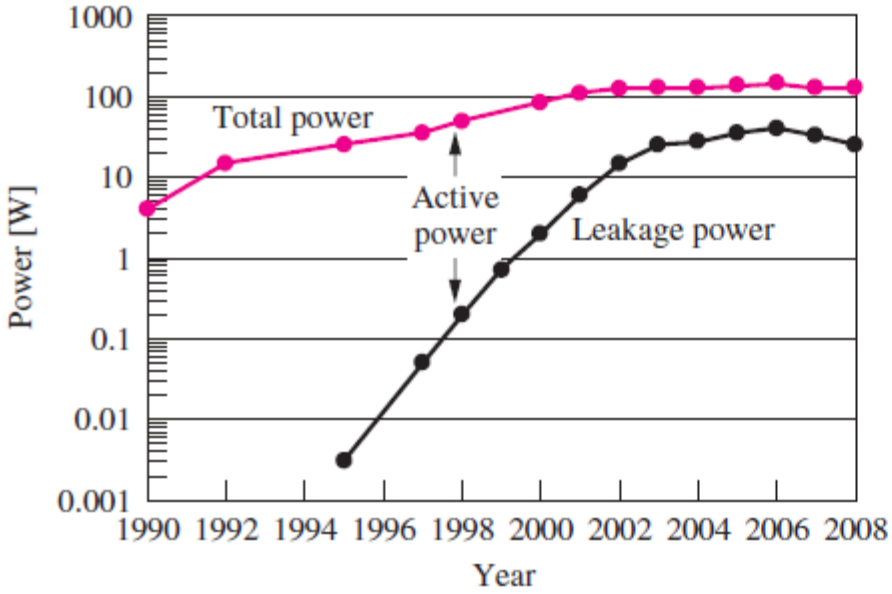
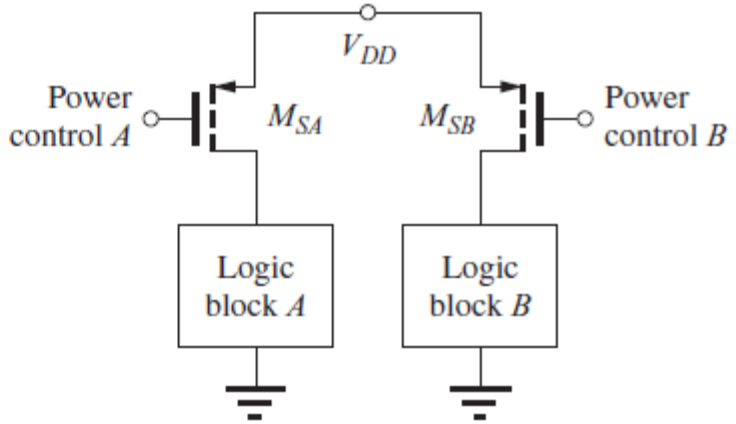


Figure 4.19 Subthreshold conduction in an NMOS transistor with $V_{TN} = 1$ V.

Power Dissipation

- V_{GS} must drop significantly below V_T to fully turn off MOSFET (lower limit on V_T ~ 0.3 V)
- Standby power significant in modern technology.

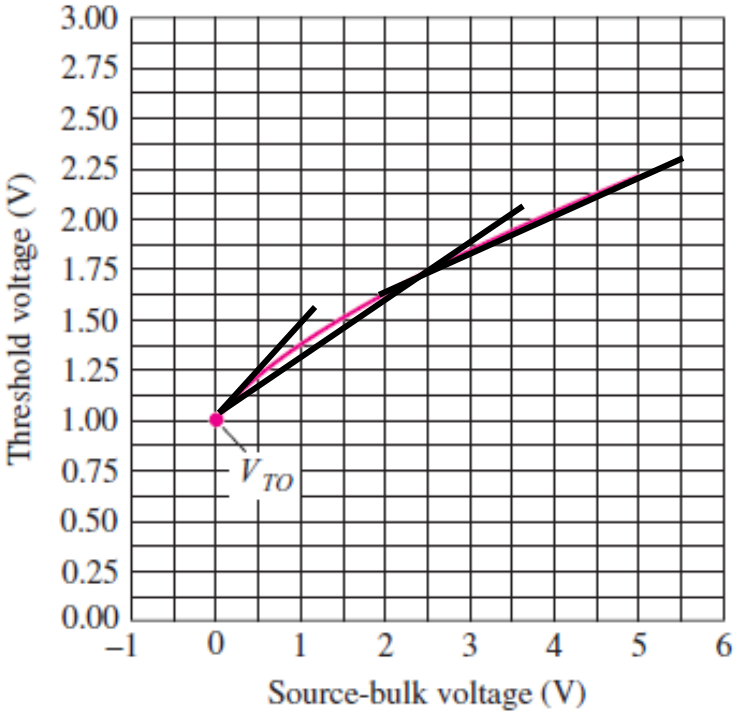


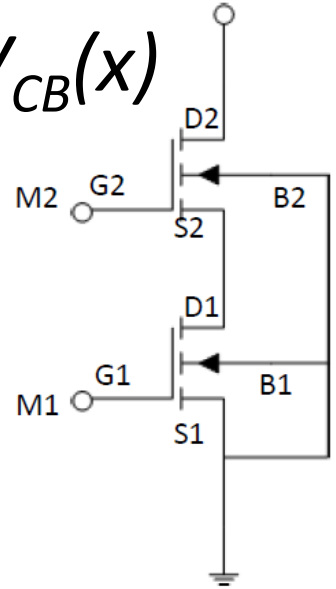


- Can turn off blocks of logic when not needed.

Distributed Body Effect

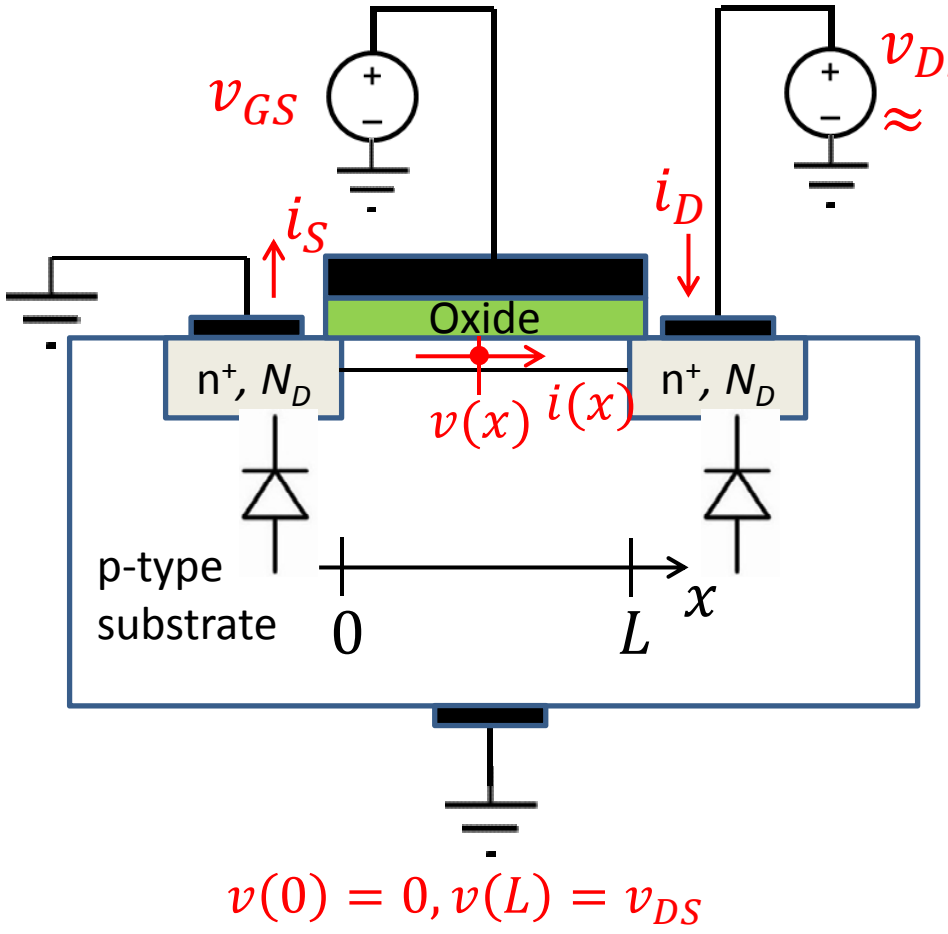
- Threshold voltage actually changes with $V_{CB}(x)$ rather than just V_{SB}.





$$V_{TN\text{eff}} = V_{TO} + \gamma\left(\sqrt{v_{CB} + 2\phi_F} - \sqrt{2\phi_F}\right)$$
$$\cong V_{TO} + \alpha v_{CB}(x)$$
$$\cong V_{TN} + \alpha v_{CS}(x)$$

n-MOSFET Analysis (Triode)



- Goal: Find $i_D = f(v_{GS}, v_{DS})$ when v_{DS} is small and $v_{SB} = 0$
- Inversion charge line density at any point in the channel:

$$Q' = -WC''_{\text{ox}}(v_{GC} - V_{TN}) = -WC''_{\text{ox}}(v_{GS} - v(x) - V_{TN}) \quad (1)$$

- Current in the channel:

$$i(x) = Q'(x)(-\mu_n E_x) \quad (2)$$

- Electric field:

$$E_x = -\frac{dv(x)}{dx} \quad (3)$$

n-MOSFET Analysis (Triode)

- Combining ①②③:

$$i(x) = -\mu_n C_{\text{ox}}'' W (v_{GS} - v(x) - [V_{TN} + \alpha v(x)]) \frac{dv(x)}{dx}$$

- Integrate between 0 and *L*: $v(0) = 0, v(L) = v_{DS}$

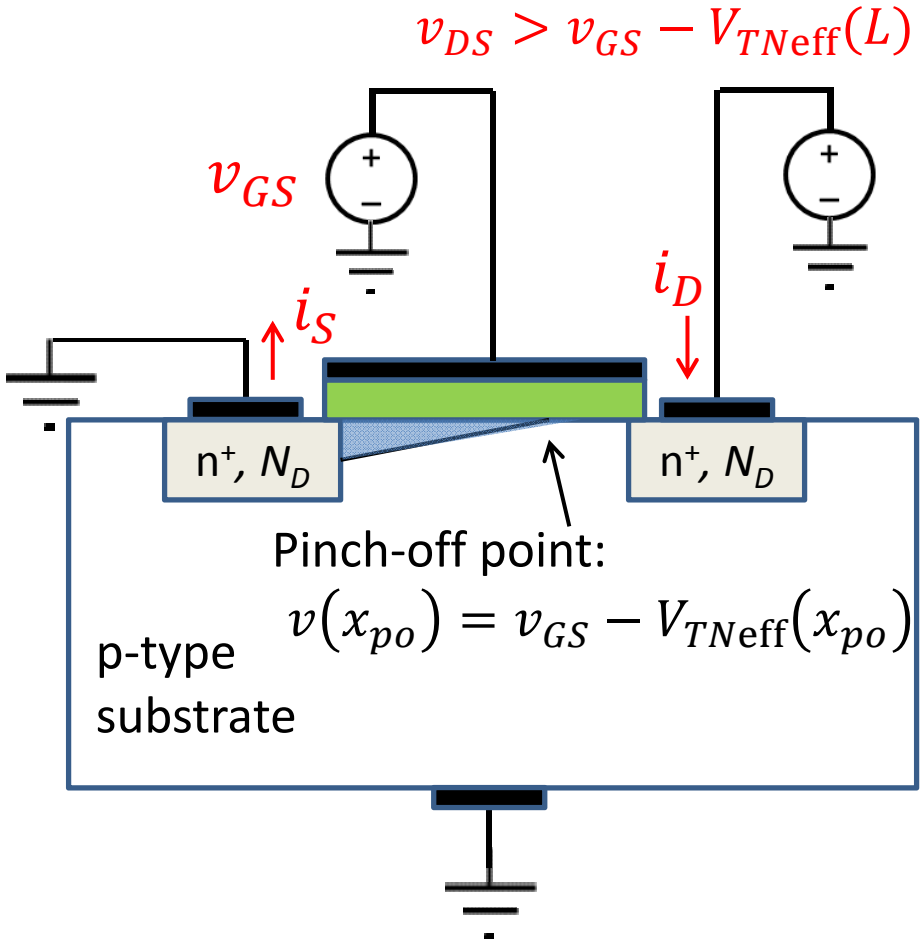
$$\int_0^L i(x)dx = \int_0^{v_{DS}} -\mu_n C_{\text{ox}}'' W (v_{GS} - [1+\alpha]v(x) - V_{TN}) dv(x)$$

- Current must be equal in the channel: $i(x) = -i_D$ Notice the sign!
- We get the triode region formula:

$$i_D = K_n' \frac{W}{L} \left(v_{GS} - V_{TN} - \frac{[1+\alpha]v_{DS}}{2} \right) v_{DS} \quad \text{where} \quad K_n' = \mu_n C_{\text{ox}}''.$$

- The channel exists as long as $v_{GC} = v_{GS} - v(x) > V_{TN\text{eff}}$ for all $0 < x < L$. This requires $v_{GS} \geq [1+\alpha]v(x)_{\max} + V_{TN} = v_{DS} + V_{TN}$
- Thus condition for triode region operation is: $v_{GS} - [1+\alpha]v_{DS} \geq V_{TN}$

Saturation (Pinch-off) region



- $v_{\text{DSAT}} = (v_{GS} - V_{TN})/[1 + \alpha]$
- $v_{DS} \geq v_{\text{DSAT}}$:

$$i_D = \frac{K_n'}{2[1+\alpha]}\frac{W}{L}(v_{GS} - V_{TN})^2$$

Example, V_{TN}=1V, α = 0.25 V^{-1}:

- V_{GS}=1V, V_{DS}=1V: cutoff
- V_{GS}=3.3V, V_{DS}=1V: linear
- V_{GS}=3.3V, V_{DS}=2V: saturation

  V_{GD}=1.3V < V_{TNeff}(L) = 1 + (0.25)2 or

  $V_{DS} > (V_{GS} - V_{TN})/(1 + \alpha)$